REMARKS

The application has been reviewed in light of the final Office Action dated April 21, 2008. Claims 19, 20, 22-40 are pending, with claims 19, 22 and 31 being in independent form.

Claims 22-24 and 30-33 were rejected under 35 U.S.C. §102(e) as purportedly anticipated by Chu et al (US 2004/0015731 A1). Claims 25, 26, 29 and 34-36 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Chu in view of U.S. Patent No. 6,470,439 to Yamada. Claims 27, 28, 37 and 38 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Chu in view of Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang. Claims 19, 20, 39 and 40 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Chu in view of U.S. Patent No. 6,528,974 to Mirov.

Chu, as understood by Applicant, proposes an approach for controlling a mode of operation of a hard disk drive (HDD), including a second mode of operation that consumes less power than a first mode of operation. In the system proposed by Chu, a power management unit (220) is interposed between a host (1) and a HDD device (2). The power management unit 220 of Chu is shown in detail in Fig. 2 reproduced below), and includes a host interface (110), a state machine (120), a write cache (130), a read cache (140), and a device interface (150). The power management unit 220 utilizes the read cache 140 and the write cache 130 to process commands from the host 1, and all read and write operations between the host 1 and the device 2 goes through power management unit 220. The state machine 120 contains logic for managing read cache 140, write cache 130, host interface 110, and device interface 150, to reduce power consumption. When the host 1 issues a data write command, the state machine 120 determines whether write cache 130 can accept the write data. If the write cache 130 can accept the data, then the data is written into write cache 130 and the power state of device 2 is unaffected.

If the write cache 130 is unable to accept the data, then the state machine 120 issues commands over device interface 150 to write the data to the device 2. When the host 1 issues a data read command, and all of the requested data is stored in the read cache 140 or the write cache 130, then the state machine 120 returns the requested data to Host 1 without affecting the power state of device 2. If any of the requested data is not stored in the read cache 140 or the write cache 130, then the state machine 120 issues the necessary read commands over device interface 150 to read the appropriate data from device 2 and send it to the host 1. Once the device 2 has satisfied the read requests, the state machine 120 is able to perform additional read operations to fill up the read cache 140, or to flush write cache 130.

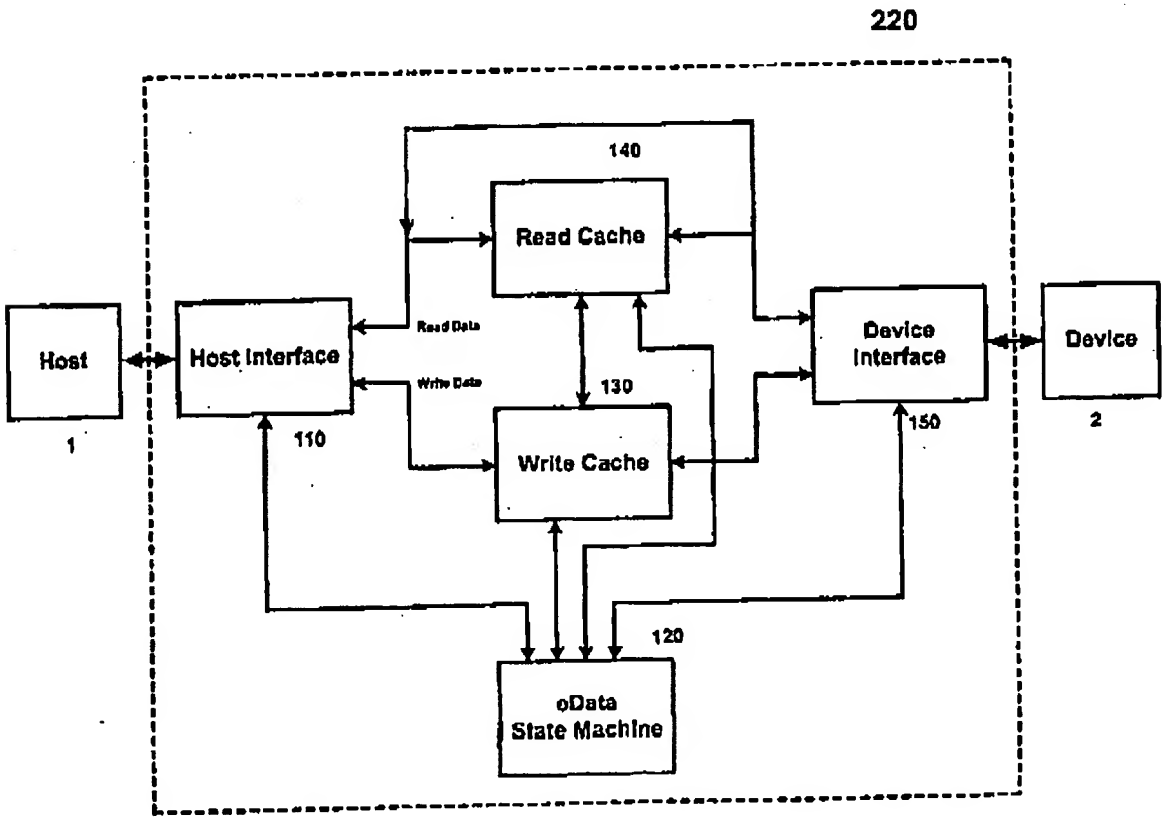

Figure 2

Fig. 3 of Chu (reproduced below) shows HDD 300. When the HDD 300 of Chu is in reduced power mode (eData mode), mechanical and electrical components are turned off, and state machine 400 controls the data transfer between host 10 and HDD 300 by electronically storing the data in RAM 420. State machine 400 configures memory 420 to include a write data buffer and various counters such as a logical block address counter, a data size counter, a cache buffer available size counter and a host data access frequency counter. When HDD 300 is operating in the eData mode and receives a read data command, state machine 400 configures memory 420 to include a read data buffer and various counters that are used for determining the optimum time for transitioning HDD 300 to Active mode for performing a read operation.

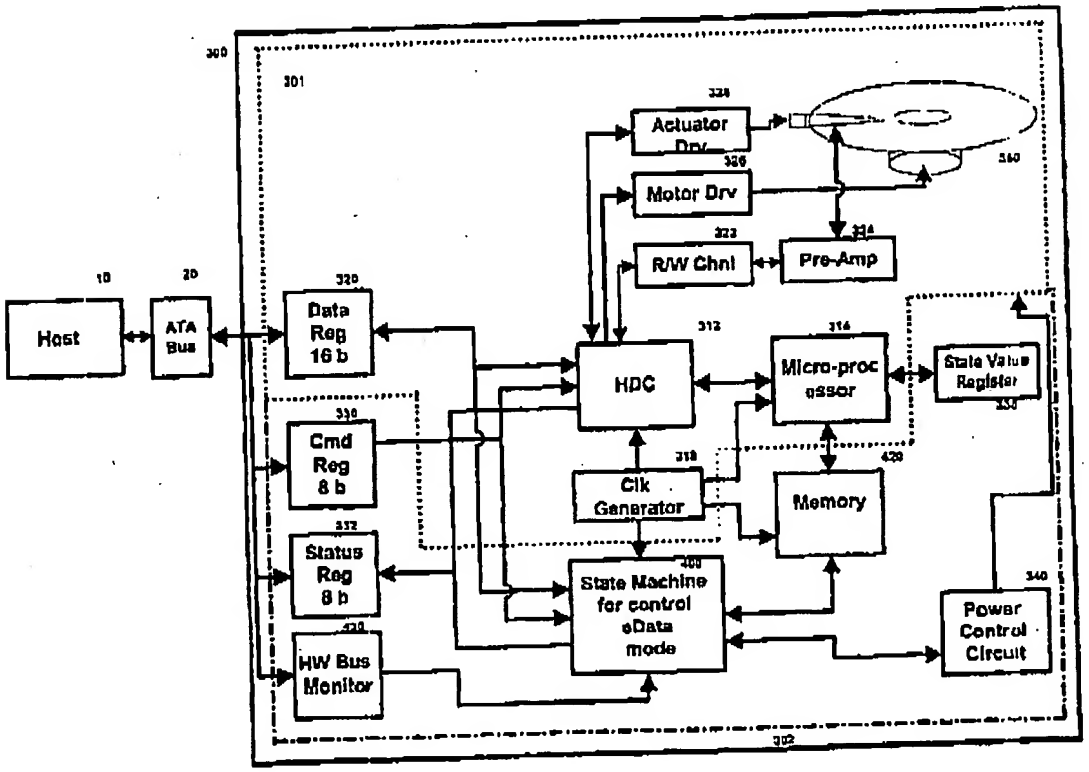

Figure 3

The 16-bit data register 320 and the memory 420 of Chu are equated in the Office Action with the register circuit and the first memory, respectively, of claim 22 of the present application. In addition, the memory 420 and state machine 400 shown in Fig. 3 of Chu are equated in the Office Action with the second memory and the control circuit, respectively, of claim 22 of the present application.

However, the 16-bit data register 320 of Chu, contrary to the contention in the Office Action, is not a register circuit including a ***plurality*** of registers.

Further, although the memory 420 of Chu can be configured to include a Logical Block Address (LBA) counter, such LBA counter has nothing to do with specific addresses of the 16-bit data register 320 of Chu. To the contrary, the LBA counter of Chu is used to store the starting address of the data in the memory 420.

Accordingly, the memory 420 of Chu does ***NOT*** store second information ***received by the memory 420 in association with first information stored in the first memory indicating specific addresses of corresponding specified registers in the register circuit***.

Further, the state machine 400 of Chu (equated in the Office Action with a control circuit) does not perform an information writing operation for writing the first information and the second information into the first memory and the second memory, respectively, ***in chronological order of accesses executed***.

Chu merely proposes that the state machine 400 uses a frequency of host data accesses to determine the most energy efficient power mode.

However, Chu says nothing whatsoever regarding performing an information writing operation for writing a first information and a second information into a first memory and a second memory, respectively, in chronological order of accesses executed.

Yamada (previously discussed in the record), Chuang (previously discussed in the record) and Mirov likewise do not disclose or suggest the above-mentioned features of independent claim 22 (and independent claim 31) of the present application.

Applicant submits that the cited art, even when considered along with common sense and common knowledge to one skilled in the art, does ***NOT*** render unpatentable the subject matter of independent claim 22 and independent claim 31 of the present application.

Accordingly, applicant submits that independent claims 22, 31 and the claims depending therefrom, are patentable over the cited art.

Regarding claim 19, the final Office Action acknowledges that Chu does not disclose or suggest an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a non-zero value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode.

In addition, Chu, contrary to the contention in the Office Action, does not disclose or suggest a path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode in which a frequency of the clock signal is reduced to a non-zero value smaller than a predetermined value. The state machine of Chu simply does not have such features. If the Examiner disagrees therewith, applicant requests the Examiner to point out by specifying paragraph and line numbers in Chu where basis for disagreement can be found.

Mirov, as understood by Applicant, proposes a power supply that is comprised of a first power module, a second power module and a controller, wherein the first power module is capable of delivering a first preselected amount of power, the second power module is capable of

delivering a second preselected amount of power, the first and second power modules can be coupled together to supply an aggregate amount of power, and the controller is adapted to selectively enable the first and second power modules to make power available in one of the first preselected amount, the second preselected amount, and the aggregate amount. Mirov further proposes that a computer system may perform its tasks at a lower clock frequency and/or with less power provided thereto without adverse impact in periods of underutilization, and in the reduced power mode, the clock frequency applied to some of the components may be reduced by a significant factor allowing the computer system to remain operational but at a reduced speed, power or capability.

While Mirov suggests reducing clock frequency in a computer system to reduce power consumption, Mirov, like Chu, does not disclose or suggest a path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode in which a frequency of the clock signal is reduced to a non-zero value smaller than a predetermined value.

Applicant submits that the cited art, even when considered along with common sense and common knowledge to one skilled in the art, does ***NOT*** render unpatentable the subject matter of claim 19 of the present application.

Accordingly, applicant submits that independent claim 19 and the claims depending therefrom are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper

should be considered to be such a petition. The Patent Office is hereby authorized to charge any required fees, and credit any overpayment, to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400